

## **REMARKS**

### **Claim Rejections**

Claims 7 and 11-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Blanchard et al. (U.S. 6,621,107). Claims 7 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tihanyi (U.S. 6,686,614). Claims 8-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tihanyi in view of Ueno et al. (U.S. 2003/015086).

### **Drawings**

It is noted that no Patent Drawing Review (Form PTO-948) was received with the outstanding Office Action. Thus, Applicant must assume that the drawings are acceptable as filed.

### **Claim Amendments**

By this Amendment, Applicant has canceled claims 1-6 and has amended claim 7 in this application. It is believed that the amended claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

Blanchard et al. teach a trench DMOS transistor with an embedded trench Schottky rectifier including one Schottky diode cell at a center (219b) and surrounded by two MOSFET trenches (219a, 219c). However, the structure of the present Application includes Schottky diode cells surrounded by a termination structure, as shown in Fig.5 and 6 of the present invention.

In claim 7 of the present invention, the first oxide layer (110) is formed on a top surface of the epi layer and the silicide layer is formed on the epi layer of those surfaces located on a lower portion of the sidewall and the bottom of the trench. As stated by the Examiner, Blanchard et al. teach the first oxide layer (210) formed on the epi-layer on the entire sidewalls and a portion of bottom of the trench around the Schottky diode cell (219b). The silicide (218) is formed in the trench but it is also

located on the insulation layer (216) and extends to the upper surface of the N+ regions (212) and P+ region (204).

Blanchard et al. do not teach a pair of trenches formed through said first oxide layer and into a top of said epi-layer and spaced from each other by a first mesa region; a termination mesa region surrounding said pair of trenches; said first mesa region and said termination mesa region are regions located on said first surface having said first oxide layer formed thereon; a Schottky barrier silicide layer formed on said epi layer located on bottom and side surfaces of said trenches; nor do Blanchard et al. teach a top metal layer acting as an anode formed on said Schottky barrier silicide layer and extended to cover all surfaces of said first mesas region and a portion of said termination mesa region.

It is submitted that Blanchard et al. do not disclose, or suggest any modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Thus, it is not believed that Blanchard et al. render obvious any of Applicant's amended claims under 35 U.S.C. § 103.

Tihanyi teaches a semiconductor switching element with an integrated Schottky diode having a have Schottky barrier silicide layer (50) only on the bottom of the trenches, and an insulation layer (74) located on sidewalls of the trench, as shown in Fig. 2.

In claim 7 of the present invention, the top metal layer (150) will be not formed on or contacted with the n+ or n- region. However, in Tihanyi, the top metal layer (60) is formed on the n+ region (10).

Tihanyi does not teach a Schottky barrier silicide layer formed on said epi layer located on bottom and side surfaces of said trenches; nor does Tihanyi teach a top metal layer acting as an anode formed on said Schottky barrier silicide layer and extended to cover all surfaces of said first mesas region and a portion of said termination mesa region.

Ueno et al. teach a semiconductor device including a semiconductor substrate (1), a drain region (2), a source region (3), stacked gate insulating regions (4a-4c), a gate electrode (5), and contact plugs (6, 7).

The stacked gate insulating regions (4a-4c) are made of a silicon oxide film (4a), a silicon nitride film (4b), and a silicon oxide film (4c). The stacked gate insulating regions in Ueno et al. are not equivalent to the first oxide layer (110) and the nitride layer (115) of the present Application, which serve as a buffer layer to relieve mechanical stress during a bonding process.

Ueno et al. do not teach a Schottky barrier silicide layer formed on said epi layer located on bottom and side surfaces of said trenches; nor do Ueno et al. teach a top metal layer acting as an anode formed on said Schottky barrier silicide layer and extended to cover all surfaces of said first mesas region and a portion of said termination mesa region.

Even if the teachings of Tihanyi, and Ueno et al. were combined, as suggested by the Examiner, the resultant combination does not suggest: a Schottky barrier silicide layer formed on said epi layer located on bottom and side surfaces of said trenches; a top metal layer acting as an anode formed on said Schottky barrier silicide layer and extended to cover all surfaces of said first mesas region and a portion of said termination mesa region.

It is a basic principle of U.S. patent law that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of Applicant's disclosure to create a hypothetical combination which allegedly renders a claim obvious, unless there is some direction in the selected prior art patents to combine the selected teachings in a manner so as to negate the patentability of the claimed subject matter. This principle was enunciated over 40 years ago by the Court of Customs and Patent Appeals in In re Rothermel and Waddell, 125 USPQ 328 (CCPA 1960) wherein the court stated, at page 331:

The examiner and the board in rejecting the appealed claims did so by what appears to us to be a piecemeal reconstruction of the prior art patents in the light of appellants' disclosure. ... It is easy now to attribute to this prior art the knowledge which was first made available by appellants and then to assume that it would have been obvious to one having the ordinary skill in the art to make these suggested reconstructions. While such a reconstruction of the art may be an alluring

way to rationalize a rejection of the claims, it is not the type of rejection which the statute authorizes.

The same conclusion was later reached by the Court of Appeals for the Federal Circuit in Orthopedic Equipment Company Inc. v. United States, 217 USPQ 193 (Fed.Cir. 1983). In that decision, the court stated, at page 199:

As has been previously explained, the available art shows each of the elements of the claims in suit. Armed with this information, would it then be non-obvious to this person of ordinary skill in the art to coordinate these elements in the same manner as the claims in suit? The difficulty which attaches to all honest attempts to answer this question can be attributed to the strong temptation to rely on hindsight while undertaking this evaluation. It is wrong to use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit. Monday morning quarterbacking is quite improper when resolving the question of non-obviousness in a court of law.

In In re Geiger, 2 USPQ2d, 1276 (Fed.Cir. 1987) the court stated, at page 1278:

We agree with appellant that the PTO has failed to establish a *prima facie* case of obviousness. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching suggestion or incentive supporting the combination.

Applicant submits that there is not the slightest suggestion in either Tihanyi, or Ueno et al. that their respective teachings may be combined as suggested by the Examiner. Case law is clear that, absent any such teaching or suggestion in the prior art, such a combination cannot be made under 35 U.S.C. § 103.

Neither Tihanyi, nor Ueno et al. disclose, or suggest a modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious Applicant's amended claims.

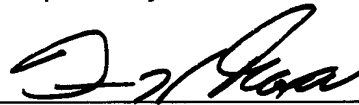
**Summary**

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

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By:



Bruce H. Troxell  
Reg. No. 26,592

TROXELL LAW OFFICE PLLC  
5205 Leesburg Pike, Suite 1404  
Falls Church, Virginia 22041  
Telephone: 703 575-2711  
Telefax: 703 575-2707